8. (Amended) The memory device of claim 7 further comprising ,on the single chip, an error detection and correction engine connected to the volatile main memory and the compression and decompression engine.

9. (Amended) A system comprising:

a processor; and

a memory device connected to the processor, the memory device comprising a volatile main memory and a compression and decompression engine connected to the volatile main memory, wherein the volatile main memory and the compression and decompression engine are located in a single chip.

11. (Amended) A system comprising:

a processor; and

a memory device connected to the processor, wherein the memory device comprises a volatile main memory, a compression and decompression engine connected to the volatile main memory , and a cache memory connected to the compression and decompression engine, wherein the volatile main memory, the compression and decompression engine, and the cache memory and are located in a single chip.

15. (Amended) A method of increasing a storage density of a memory device, the method comprising:

providing a volatile main memory;

providing a compression and decompression engine; and

connecting the compression and decompression engine to the volatile main memory, wherein the volatile main memory and the compression and decompression engine are located in a single chip.

18. (Amended) A method of operating a memory device, comprising:

receiving input data at a cache memory;

compressing the input data at a compression and decompression engine to produce compressed data; and

storing the compressed data into a volatile main memory, wherein the cache memory, the compression and decompression engine, and the volatile main memory are located in a single chip.

19. (Amended) The method of claim 18 further comprising:

reading the compressed data from the volatile main memory;

decompressing the compressed data at the compression and decompression engine to produced decompressed data; and

reading the decompressed data to the cache memory.

20. (Amended) A method of operating a memory device, comprising:

receiving data at an input/output buffer;

processing the data at a cache memory to produce processed data;

compressing the processed data at a compression and decompression engine to produce compressed data; and

storing the compressed data into a volatile main memory , wherein the input/output buffer, the cache memory, the compression and decompression engine, and the volatile main memory are located in a single chip.

21. (Amended) The method of claim 20 further comprising:

reading the compressed data from the volatile main memory;

decompressing the compressed data at the compression and decompression engine to produced decompressed data;

reading the decompressed data at the cache memory; and

transferring the data to the input/output buffer.